REMARKS

This amendment is submitted in response to an Office Action mailed August 18, 2006. Applicant respectfully requests reconsideration of the subject application as amended herein.

Claims 21 and 35 have been cancelled without prejudice. Claims 1-20, 22-34, and 36-41 remain in the present application.

In the August 18, 2006 Office Action, claims 1-41 were rejected under 35 U.S.C. § 102 or 103 as being anticipated by or obvious over various combinations of one or more of the following (collectively referred to hereinafter as "the cited references"):

U.S. Patent No. 6,385,735 issued to Wilson et al. (hereinafter "Wilson")

U.S. Patent No. 6,175,929 issued to Hsu et al. (hereinafter "Hsu");

U.S. Patent No. 6,691,242 issued to Pollock et al. (hereinafter "Pollock"); and

U.S. Patent No. 6,073,249 issued to Watabe et al. (hereinafter "Watabe").

Claims 21 and 35 have been cancelled, rendering the rejections of such claims moot.

Applicant has amended the remaining claims to clearly distinguish over the cited references. For example, amended claim 1 now reads as follows:

> An apparatus comprising:
> a memory element in a processor to supply a configured clock rate setting for use by a peripheral set;
> an input element in the processor to receive a feedback clock rate setting from the peripheral set, said feedback clock rate setting being bundled with a plurality of power-on-configuration (POC) signals received in response to a reset of the processor; and
> a comparison unit in the processor to compare the configured clock rate setting and the feedback clock rate setting to detect over-clocking of the processor.

In amended claim 1, when a processor is reset, the processor tells a peripheral set what the clock setting is for the processor. The peripheral set is expected to echo that clock setting back to the processor along with power-on-configuration (POC) signals that are generated in response to the reset. In other words, the clock information is bundled into the POC signals. If the echoed clock setting is not the expected setting (less-than-or-equal-to, for instance), the comparison unit can detect over-clocking.

WILSON

In contrast, Wilson describes frequency select signals 16 that can be set by configuring jumpers on a motherboard or through software programming using the Basic Input Output System (BIOS) (Wilson: col. 2, lines 53-62; col. 3, line 64 to col. 5, line 3). In either case, the frequency select signals 16 are simply provided to the processor for comparison to a maximum processor clock frequency (Wilson: col. 4, lines 51-55; col. 4, line 64 to col. 5, line 4).

Applicant respectfully submits that Wilson does not describe echoing clock setting data back to a processor, much less any particular mechanism for delivering the echoed data to the processor.

Therefore, Applicant respectfully submits that Wilson does not suggest, disclose, or enable "an input element in the processor to receive a feedback clock rate setting from the peripheral set, said feedback clock rate setting being bundled with a plurality of power-on-configuration (POC) signals received in response to a reset of the processor," as claimed in amended claim 1.

HSU

Hsu was cited for disclosing "that the processor is in charge of the operation of the entire computer main board and the processor communicates with peripherals about the clock frequency" (August 18, 2006 Office Action, page 3, 2nd paragraph). Assuming for the sake of argument that the Office Action is correct with respect to the teachings of Hsu, Applicant respectfully submits that

Hsu includes nothing whatsoever about power-on-configuration (POC) signals received by a processor in response to a reset, much less bundling echoed clock setting data with the POC signals.

Thus, Applicant respectfully submits that Hsu fails to cure the deficiencies of Wilson as discussed above.

POLLOCK

Pollock was cited under 35 U.S.C. § 103 in combination with Wilson and Hsu. Pollock, however, was published Feb 10, 2004, after the September 15, 2003 filing date of the present application. Therefore, Pollock is 102(e)-type prior art. Furthermore, Pollock and the present application have a common assignee, Intel Corporation, and the present application was assigned, or subject to an obligation to assign, to the common assignee at the time of invention. Therefore, Pollock is unavailable as prior art under 35 U.S.C. § 103(C)(1).

WATABE

Watabe was cited for disclosing the "use of a tri-state unit and a logic AND" (August 18, 2006 Office Action, page 11, paragraph 27). Assuming for the sake of argument that the Office Action is correct with respect to the teachings of Watabe, Applicant respectfully submits that Watabe includes nothing whatsoever about power-on-configuration (POC) signals received by a processor in response to a reset, much less bundling echoed clock setting data with the POC signals.

Thus, Applicant respectfully submits that Watabe fails to cure the deficiencies of Wilson as discussed above.

CONCLUSION

As discussed above, Applicant respectfully submits that the cited references, either alone or combined, do not suggest, disclose, or enable "a feedback clock rate setting from the peripheral set" for a processor, "said feedback clock rate setting being bundled with a plurality of power-on-

configuration (POC) signals ... in response to a reset of the processor," as claimed in amended claim 1.

Thus, for at least the reasons discussed above, Applicant respectfully submits that amended claim 1 is patentable over the cited references.

Applicant submits that the reasoning presented above with respect to amended claim 1 similarly applies to claims 2-20, 22-34, and 36-41. Thus, for at least the reasons discussed above, Applicant respectfully submits that claims 2-20, 22-34, and 36-41 are likewise patentable over the cited references.

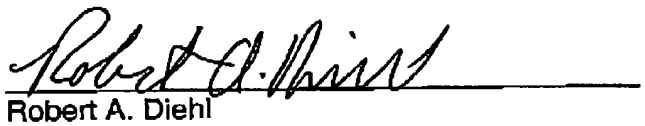
In conclusion, Applicant respectfully submits that claims 1-20, 22-34, and 36-41 are now in a condition for allowance, and Applicant respectfully requests allowance of such claims.

Please charge any shortages and credit any overages to our Deposit Account No. 50-0221.

Respectfully submitted,

INTEL CORPORATION

Date: Nov 20, 2006



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